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Indian Standard

SEMICONDUCTOR DEVICES — INTEGRATED CIRCUITS — GENERIC SPECIFICATION FOR FILM INTEGRATED CIRCUITS AND HYBRID FILM INTEGRATED CIRCUITS

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Indian Standard

SEMICONDUCTOR DEVICES — INTEGRATED CIRCUITS — GENERIC SPECIFICATION FOR FILM INTEGRATED CIRCUITS AND HYBRID FILM INTEGRATED CIRCUITS

NATIONAL FOREWORD

This Indian Standard, which is identical with IEC Pub 747-20/QC 760000 (1988) 'Semiconductor devices — Integrated circuits — Part 20 : Generic specification for film integrated circuits and hybrid film integrated circuits', issued by the International Electrotechnical Commission (IEC), was adopted by the Bureau of Indian Standards on the recommendation of the Semiconductor Devices and Integrated Circuits Sectional Committee (LT 10) and approval of the Electronics and Telecommunication Division Council.

The text of IEC standard has been approved as suitable for publication as Indian Standard without deviations. Certain conventions are, however, not identical to those used in Indian Standards. Attention is particularly drawn to the following:

> Wherever the words 'International Standard' appear referring to this standard, they should be read as 'Indian Standard'.

In this adopted standard, reference appears to certain International Standards for which Indian Standards also exist. The corresponding Indian Standards which are to be substituted in their place are listed below along with their degree of equivalence for the editions indicated:

International Standard	*Corresponding Indian Standard*	*Degree of Equivalence*
IEC QC 001001 : 1886	IS QC 001001 : 1988 Basic rules of IEC quality assessment system for electronic components (IECQ)	Identical
IEC QC 001002 : 1986	IS QC 001002 : 1988 Rules of procedure IEC quality assessment system for electronic components (IECQ)	Identical

The concerned technical committee has reviewed the provisions of IEC Pub 27-1, IEC Pub 50, IEC Pub 68-1, IEC Pub 68-2-1, IEC Pub 68-2-1A, IEC Pub 68-2-2, IEC Pub 68-2-2A, IEC Pub 68-2-3, IEC Pub 68-2-6, IEC Pub 68-2-7, IEC Pub 68-2-11, IEC Pub 68-2-14, IEC Pub 68-2-17, IEC Pub 68-2-20, IEC Pub 68-2-21, IEC Pub 68-2-27, IEC Pub 68-2-30, IEC Pub 68-2-45, IEC Pub 68-3-1, IEC Pub 191-1, IEC Pub 191-2, IEC Pub 191-3 IEC Pub 410, IEC Pub 695-2-2, IEC Pub 747-1, IEC Pub 748-1 and IEC Pub 749, referred in this adopted standard and has decided that they are acceptable for use in conjunction with this standard.

This standard is intended primarily for use under the IECQ system. A regular Indian Standard for this component could be different, identical or similar to this standard.

Only the English language text in the International Standard has been retained while adopting it as Indian Standard.

As in the Original Standard, this Page is Intentionally Left Blank

SECTION 1 - SCOPE, OBJECT AND CLASSIFICATION

1.1 Scope

This generic specification is applicable to film integrated circuits and to hybrid film integrated circuits (F and HFICs), both passive and active, as in IEC Publication 748-1, Chapter IV, Sub-clause 2.4.

It applies also to partly-completed F and HFICs supplied to customers for subsequent processing. This specification also applies to chip carrier circuits having more than one chip, provided that they, as separate products, have been interconnected by film interconnection techniques.

This specification is not intended to cover printed circuit boards but is applicable to F and HFICs which may include them.

1.2 Object

This specification defines the quality assessment procedures and the methods for electrical, climatic, mechanical and endurance tests.

It outlines the requirements which shall be applied to the release of circuits using either qualification approval procedures or capability approval procedures. The requirements of these procedures are given in Clauses 3.5 and 3.6 respectively.

1.3 Technological classification of F and HFICs

F and HFICs are classified according to their structure and technology of manufacture as shown in Table I.

Table I

Film	1) Thick film 2) Thin film 3) Other
Circuit structure	1) Passive thin and thick film circuits 2) Active thin and thick film circuits 3) Hybrid film integrated circuits 4) Multiple substrate combinations
Added components	0) None 1) All types of passive and/or encapsulated active devices 2) All types of passive and active devices including unencapsulated semiconductor dice
Circuit encapsulation	1) None 2) Embedded 3) Cavity with any organic seal or wall 4) Cavity with inorganic seal and walls

SECTION 2 - GENERAL

2.1 Order of precedence

Where any discrepancies occur for any reason, documents shall rank in the following order of precedence:

- the detail specification;
- the sectional specification;
- the generic specification;
- rules of procedure (IECQ), IEC Publication QC 001002;
- basic rules (IECQ), IEC Publication QC 001001;
- any other international documents, for example IEC publications to which reference is made.

The same order of precedence shall apply to equivalent national documents.

2.2 Related documents

The detail specification shall indicate the applicable documents.

IEC publications:

Publication 27-1 (1971):	Letter symbols to be used in electrical technology, Part 1: General.
50.	International Electrotechnical Vocabulary (IEV).
68:	Basic environmental testing procedures.
68-1 (1982):	Part 1: General and guidance.
68-2:	Part 2: Tests.
68-2-1 (1974):	Tests A: Cold.
68-2-1A (1976):	First supplement to Publication 68-2-1 (1974).
68-2-2 (1974):	Tests B: Dry heat.
68-2-2A (1976):	first supplement to Publication 68-2-2 (1974).
68-2-3 (1969):	Test Ca: Damp heat, steady state.
68-2-6 (1982):	Test Fc and guidance: Vibration (sinusoidal).
68-2-7 (1983):	Test Ga and guidance: Acceleration, steady state.
68-2-11 (1981):	Test Ka: Salt mist.
68-2-14 (1984):	Test N: Change of temperature.
68-2-17 (1978):	Test Q: Sealing.
68-2-20 (1979):	Test T: Soldering.
68-2-21 (1983):	Test U: Robustness of terminations and integral mounting devices.
68-2-27 (1972):	Test Ea: Shock.
68-2-30 (1980):	Test Db and guidance: Damp heat, cyclic (12 + 12-hour cycle).
68-2-45 (1980):	Test XA and guidance: Immersion in cleaning solvents.
68-3-1 (1974):	Part 3: Background information, Section One - cold and dry heat tests.
191-1 (1966):	Mechanical standardization of semiconductor devices. Part 1: Preparation of drawings of semiconductor devices.

191-2 (1966):	Part 2: Dimensions.
191-3 (1974):	Part 3: General rules for the preparation of outline drawings of integrated circuits.
410 (1973):	Sampling plans and procedures for inspection by attributes.
695-2-2 (1980):	Fire hazard testing, Part 2: Test methods. Needle-flame test.
747-1 (1983):	Semiconductor devices. Discrete devices and integrated circuits, Part 1: General.
748-1 (1984):	Semiconductor devices. Integrated circuits, Part 1: General.
749 (1984):	Mechanical and climatic test methods.
QC 001001 (1986):	Basic rules for the IEC quality assessment system for electronic components (IECQ).
QC 001002 (1986):	Rules of procedure of the IEC quality assessment system for electronic components (IECQ).

2.3 Units and symbols

Units, graphical symbols and letter symbols shall, whenever possible, be taken from the following publications:

IEC Publication 27:	Letter symbols to be used in electrical technology.
IEC Publication 617:	Graphical symbols for diagrams.
ISO Standard 1000 (1981):	SI units and recommendations for the use of their multiples and of certain other units.

Any other units and symbols required shall be derived in accordance with the principles of the publications listed above.

2.4 Terminology (for information)

Terminology shall, wherever possible, be taken from:

IEC Publication 50: International Electrotechnical Vocabulary (IEV).

Any other terminology required should be derived in accordance with the principles of this publication.

2.4.1 *Microelectronics* (IEC 748-1)

The concept of the construction and use of highly miniaturized electronic circuits.

2.4.2 *Microcircuit* (IEC 748-1)

A microelectronic device, having a high equivalent circuit-element and/or component density, which is considered as a single unit.

Note.- A microcircuit may be a micro-assembly or an integrated (micro)circuit.

2.4.3 *Integrated circuit* (IEC 748-1 modified)

A circuit in which a number of circuit elements are inseparably associated and electrically interconnected such that, for the purpose of specification, testing, commerce and maintenance, it is considered indivisible.

Note.- For this definition, a circuit element does not have an envelope or external connection and is not specified or sold as a separate item.

2.4.4 *Integrated microcircuit* (IEC 748-1 modified)

A microcircuit in which a number of circuit elements are inseparably associated and electrically interconnected such that, for the purpose of specification and testing and commerce and maintenance, it is considered indivisible.

Notes 1.- For this definition, a circuit element does not have an envelope or external connection and is not specified or sold as a separate item.

2.- Where no misunderstanding is possible, the term "integrated microcircuit" may be abbreviated to "integrated circuit".

3.- Further qualifying terms may be used to describe the technique used in the manufacture of a specific integrated microcircuit.

Examples of use of qualifying terms:

- semiconductor monolithic integrated circuit;
- semiconductor multi-chip integrated circuit:
- thin film integrated circuit;
- thick film integrated circuit;
- hybrid integrated circuit.

2.4.5 *Micro-assembly* (IEC 748-1 modified)

A microcircuit consisting of various components and/or integrated micro-circuits which are constructed separately and which can be tested before being assembled and packaged.

Notes *1.*- For this definition, a component has external connections and possibly an envelope as well and it can also be specified and sold as a separate item.

2.- Further qualifying terms may be used to describe the form of the components and/or the assembly techniques used in the construction of a specific micro-assembly.

Examples of use of qualifying terms:

- semiconductor multi-chip micro-assembly;
- discrete component micro-assembly.

2.4.6 *Semiconductor integrated circuit* (IEV 521-10-06 modified)

An integrated circuit whose elements and interconnections are formed within and upon a semiconductor.

2.4.7 *Multichip microcircuit*

A microcircuit containing chip components for surface mounting which are separately mounted upon a substrate.

2.4.8 *Film*

A layer of solid formed by any deposition process in-situ upon a solid substrate.

2.4.9 *Foil*

A solid film which can be handled independent of a substrate.

2.4.10 *Thin film*

A film deposited upon a substrate by an accretion process such as vacuum evaporation, sputtering and chemical vapour deposition.

2.4.11 *Thick film*

A film deposited upon a substrate, usually by a screen printing process.

2.4.12 *Film integrated circuit*

An integrated circuit whose elements and interconnections are films formed on an insulating substrate surface. The film elements may be active or passive.

2.4.13 *Hybrid integrated circuit*

An integrated circuit formed by any combination of semiconductor and film integrated circuits or by the combination of any of these circuits with discrete elements.

2.4.14 *Hybrid film integrated circuit*

A film integrated circuit on which at least one component, encapsulated or unencapsulated, has been mounted.

2.4.15 *Passive hybrid film integrated circuit*

A hybrid film integrated circuit in which all the elements are passive.

2.4.16 *Active hybrid film integrated circuit*

A hybrid film integrated circuit in which at least one element is active.

2.4.17 *Semiconductor chip hybrid film integrated circuit*

A hybrid film integrated circuit containing one or more unencapsulated semiconductor devices.

2.4.18 *Substrate*

A piece of material forming a supporting base for film circuit elements and/or added components.

2.4.19 *Multilayer film circuit*

A circuit of more than one layer of film interconnection, separated by at least one insulating film or gap.

2.4.20 *Circuit element*

An element, passive or active, of an integrated circuit that performs an electrical function.

2.4.21 *Active element*

An element primarily contributing electrical rectification, switching or gain to a circuit function.

Note.- Active elements may also be used to contribute resistance and capacitance to a circuit function, or to convert externally applied energy from one form to another.

Examples are diodes, transistors, semiconductor integrated circuits, light-sensing and light-emitting semiconductor devices.

2.4.22 *Passive element*

An element primarily contributing resistance, capacitance or inductance or a combination of these to a circuit function.

Note.- Examples are resistors, capacitors, inductors, filters, interconnecting tracks.

2.4.23 *Thin-film integrated circuit* (IEV 521-10-08)

A film integrated circuit whose films are formed by vacuum deposition techniques, possibly supplemented by other deposition techniques.

2.4.24 *Thick-film integrated circuit* (IEV 521-10-09)

A film integrated circuit whose films are formed by printing, serigraphy or other related techniques.

2.4.25 *Vapour phase deposition technique*

The deposition of conducting, insulating or semiconducting films onto solid substrates from a source material in the vapour phase by physical deposition or chemical reaction.

2.4.26 *Screen printing technique*

The deposition of films onto substrates by pressing pastes (inks) through screens.

2.4.27 *Plated film*

Film obtained through chemical and/or electrochemical deposition.

2.4.28 *Termination (terminal)*

Conductor (pin, tab, pad, etc.) providing external electrical access to the integrated circuit.

2.4.29 *Package*

Total or partial envelope of an integrated circuit which provides:

- mechanical protection;
- environmental protection;
- outline dimensions.

The package may also contain or provide terminations. It contributes to the thermal characteristics of the integrated circuit.

2.4.30 *Encapsulation*

Encapsulation is the general process of surrounding the circuit or components with a protection medium against mechanical and physical/chemical stresses.

2.4.31 *Protective coating*

A layer of insulating material applied over the circuit elements for the purpose of mechanical protection and prevention of contamination.

2.4.32 *Embedding*

A process using resins which can be hardened to produce a body embedding the electronic assembly, for example:

- casting;
- potting;
- dip-coating;
- transfer moulding.

2.4.33 *Process test vehicle*

A specimen, not necessarily of a circuit but representative of at least one operation in the production line for the circuit to be qualified, and on which tests can be carried out to validate control of one or more processes.

2.4.34 *Capability qualifying circuit (CQC)*

A test specimen used to assess, in part or in whole, a declared capability. It may be either a specially designed test specimen or a normal production circuit, or a combination of both.

2.4.35 *Partly completed component of F and HFICs*

A component of F and HFICs taken uncompleted from its production line. It cannot be used for complete assessment to the specification applicable in its normal finished state.

2.4.36 *Added component*

A component which is connected mechanically and electrically to a substrate.

2.4.37 *Screening*

Examination or testing applied to all products in a lot for the purpose of detecting and removing potential failures.

2.4.38 *Assessment level*

Reflects the degree of assurance the purchaser has that the circuit meets the specification. It also indicates the balance between lot by lot and periodic testing and severity of the inspection level and AQLs of the sampling plans.

2.5 Standard and preferred values

Values should preferably be chosen from the following list:

- dimensions: IEC Publication 191-2;
- preferred temperatures (°C) are: -65, -55, -40, -25, -10, +5, +25, +40, +55, +70, +85, +100, +125, +155.

2.6 Marking

2.6.1 The information given in the marking is selected from the following list; the relative importance of each item is indicated by its position in the list:

1) terminal identification (e.g. position of pin No. 1);

2) type designation;

3) date code;

4) factory identification code;

5) manufacturer's name or trade mark;

6) mark of conformity (unless a certificate of conformity is used);

7) special handling and safety precautions.

2.6.2 The circuits shall be clearly marked with Items 1), 2) and 3) above and with as many as possible of the remaining items as is considered necessary.

Any duplication of information in the marking of the circuits should be avoided.

2.6.3 The primary package containing the circuits shall be clearly marked with the relevant information from Sub-clause 2.6.1.

2.6.4 Any additional marking shall be so applied that no confusion can arise.

SECTION 3 - QUALITY ASSESSMENT PROCEDURES

3.1 Primary stage of manufacture

The primary stage of manufacture is the production of the first layer on the surface of a substrate.

3.2 Manufacturing stages and sub-contracting

3.2.1 *Manufacturing stages in a factory of an approved manufacturer in a non-IEC member country*

a) Circuits manufactured by an approved manufacturer in a factory of his company in a non-IEC member country can be delivered under the system only if the conditions of IEC Publication QC 001002, Sub-clause 10.3, are met.

b) The sectional specification shall indicate if, for technical reasons only, the principle of extension of manufacturer's approval shall not be applied for a given sub-family or type of circuit.

3.2.2 *Sub-contracting of manufacturing processes*

Circuits that are partly manufactured in a factory other than the approved manufacturer's can be delivered under the system only when the conditions of IEC QC 001002, Sub-clauses 10.3 and 11.1.2, are met.

The sub-contracted processes may be either the film production, or one or two of the following:

- trimming of elements;
  mounting of components;
  encapsulation.

Where the initial design of the film layout has been made by a customer or a third party by agreement with the approved manufacturer, the latter is responsible for ensuring that it complies with his design rules and for taking any necessary corrective action. This responsibility shall not be sub-contracted.

3.3 Manufacturer approval

To obtain manufacturing approval the manufacturer shall meet the rules of IEC Publication QC 001002 and shall state the technological class(es) for which he seeks approval according to Table I of Section 1.

3.4 Approval of film integrated circuits and hybrid film integrated circuits

3.4.1 *Approval procedures*

To qualify a circuit, either as a custom-built or as a standard/catalogue item, either of the following two procedures may be used. These procedures conform to those stated in IEC Publication QC 001002, Clause 11.

To cover the different requirements of various electronics market sectors, three assessment levels (K,L,M) are specified for approval as described in the sectional specification. Assessment level M is the minimum mandatory level; assessment level L is higher with larger sample sizes and assessment level K is the highest level, requiring even larger sizes and also specifying screening tests.

1) *Qualification approval*

   The programme of tests for the appropriate assessment and severity level applied directly to the circuit to be qualified, as prescribed in Sub-clause 3.5 and the relevant sectional specification.

2) *Capability approval*

   The circuits and capability qualifying circuits (CQCs) are tested in combination and approval given to a manufacturing facility on the basis of validated design rules, processes and quality control procedures, as prescribed in Clause 3.6 and the relevant sectional specification.

   Note.- With capability approval, in addition to the testing of circuits, the manufacturer specifies in a capability manual his procedures for design, materials and processes and accepts monitoring of these by the National Supervising Inspectorate (NSI). Control is exercised by the combination of the lot-by-lot tests on all circuits released, together with periodic tests on capability qualifying circuits (CQCs) and, if applicable, together with tests on process vehicles, to validate the capability on a routine basis.

Capability approval is usually convenient when structurally similar circuits based on common design rules are fabricated, in small or large quantities, by a group of common processes, even though they may have different electrical functions.

It the case of custom-built circuits, the customer and manufacturer will agree upon the detail specification.

3.4.2 *Detail specifications*

The detail specifications may introduce additional tests and/or tighter inspection plans than those given in the relevant sectional specification. They shall not, however, relax the requirements of the generic specification and the relevant sectional specifications.

The detail specification and certificate of conformity shall indicate whether the qualification approval procedure or the capability approval procedure has been used and which level of assessment has been applied.

3.5 Qualification approval

3.5.1 *Granting of qualification approval*

3.5.1.1 When using the method given in Item *a)* of IEC Publication QC 001002, Sub-clause 11.3.1, a circuit is qualified to a certain assessment level (K,L,M) after successful completion of the full programme of tests for qualification approval.

3.5.1.2 When using the method given in Item *b)* of IEC Publication QC 001002, Sub-clause 11.3.1, a circuit is qualified after successful completion of the full programme for lot-by-lot tests on three inspection lots and one lot for periodic inspection (quality conformance inspection).

3.5.2 *Maintenance of qualification approval*

3.5.2.1 Qualification approval is maintained after successful completion of the procedures and requirements of quality conformance inspection (see Sub-clause 3.5.1.2).

3.5.2.2 The manufacturer shall also have maintained continuous production, for example:

a) there has been no change in the place of manufacture and final test;

b) there has been no break exceeding two years in the manufacturer's declared periodic test schedule (see Table III of the relevant sectional specification).

3.5.3 *Structural similarity*

The grouping of structurally similar circuits for the purpose of qualification approval and quality conformance inspection shall be prescribed in the relevant sectional specification.

3.5.4 *Materials, piece parts and components*

Materials, piece parts and components other than those approved under the IECQ System, may also be used provided the Chief Inspector is satisfied as to their conformance to the relevant specification and that the quality of the completed circuits shall not be reduced by their use. This is achieved by:

a) the provision of adequate procurement documents, and

b) the application of adequate vendor assessment, control procedures and acceptance tests.

The NSI shall have access to the data on which the Chief Inspector has based his acceptance of these items.

3.5.5 *Changes in manufacturing approval*

It is the responsibility of the Chief Inspector to decide whether a change in the manufacturing approval is classified as a "major" one.

A record of all changes in materials and/or manufacturing procedures which may affect the quality of the approved circuits shall be maintained. These data shall be made available to the NSI on request.

3.5.5.1 *Major changes*

Where a change is required which significantly affects the quality of the approved circuit, an incremental validation test programme based on Table I of the appropriate sectional specification shall be agreed with the NSI. Upon its successful completion, the relevant specification(s) shall be amended as necessary.

3.5.5.2 *Other changes*

Where the change is considered to be "not major", no formal approval tests are required though the chief inspector may, at his discretion, request supporting data or tests to satisfy himself.

3.6 Capability approval

3.6.1 *Capability*

3.6.1.1 *General*

A capability in any stated F and HFIc technology consists of:

a) the complete design, material preparation and manufacturing sequences, including control procedures and tests;

b) the performance limits claimed for the processes and circuits, that is, those specified for the CQCs and any other relevant test vehicles;

c) the range of mechanical structures for which approval is granted;

d) the range of added components used.

From time to time, a capability may be extended or reduced to suit the forecast needs of the manufacturer. The NSI shall be advised of all major changes (Sub-clause 3.6.3.5).

A capability manual shall be prepared by the manufacturer in accordance with Sub-clause 3.6.4.

3.6.1.2 *Limits of capability*

Included are all guaranteed performance limits identified by the manufacturer in his capability manual as applicable to his designs, film elements and finished circuits.

These shall be assessed periodically in accordance with Sub-clause 3.6.3 and the latest issue of the capability manual.

3.6.2 *Added components*

All added components shall be purchased, inspected and tested in accordance with the procedures given in the capability manual.

The manufacturer's Chief Inspector shall be satisfied as to their conformance with the relevant component specification and that the quality of the final circuits shall not be reduced by their use. The NSI shall have access to the data on which he has based his acceptance of added components.

3.6.2.1 *Qualified components*

IEC approved components may be incorporated without specific testing.

3.6.2.2 *Non-qualified components*

Added components can obtain "qualified" status when they receive a supplementary assessment applied in an IECQ country by one of the following methods:

a) Testing by the user or other approved manufacturer or test house in accordance with an appropriate IECQ specification or if not available an equivalent national specification of an IECQ country. This method is mandatory for assessment level K.

b) Testing within CQCs in accordance with test schedules for capability approval, lot-by-lot and periodic testing of the sectional specification. Structural similarity rules of the appropriate IECQ component specification apply.

c) Testing within CQCs in accordance with test schedules for capability approval, lot-by-lot and periodic testing of the sectional specification. Structural similarity rules of the sectional specification apply.

Additional lot-by-lot tests on completed circuits containing them, comprising:

i) 100%: change of temperature;
5 cycles between maximum and minimum storage temperature;

ii) 100%: Endurance for 168^{0}_{-8} h;

iii) 100%:Static and dynamic characteristics at room temperature.

3.6.2.2.1 *Added components having "non-qualified" status*

These components may be used subject to the requirements of Sub-clause 3.6.2.3.

In the case of unencapsulated semiconductor dice, they shall be subjected to visual inspection in accordance with the relevant specification at Inspection Level (IL) S2, Acceptable Quality Level (AQL), 1.5%.

3.6.2.3 *Added components and circuit assessment levels*

For the release of circuits to assessment levels K, L or M, added components of "qualified" or "non-qualified" status may be used, subject to the following criteria:

a) When the circuits contain components all of "qualified" status, the assessment levels may be stated as K, L or M.

b) When the circuits contain one or more components of "non-qualified" status, the circuit detail specification shall:

- identify the assessment levels as L/N or M/N as applicable,

and

- list all those added components which have "non-qualified" status.

3.6.3 *Capability approval procedures*

3.6.3.1 *Granting of capability approval*

To obtain capability approval the manufacturer shall:

a) apply the rules given in IEC Publication QC 001002, Sub-clause 11.7;

b) prepare a capability manual in accordance with Sub-clause 3.6.4 of this specification;

c) satisfy the NSI that the selection of CQCs is representative of the circuits to be released in accordance with the structural similarity rules prescribed in the sectional specification and that it fully assesses all the capability boundaries, the range of materials and components (including sources used) and the range of products claimed in the capability manual;

d) declare to the NSI the test schedule and the relevant test severities for capability approval testing;

e) carry out the test programme in accordance with capability approval testing and the manufacturer's related CQC specifications and any relevant process test vehicle specification;

f) submit the test results to the NSI for approval;

g) prepare a capability approval report containing the following information:

  i) reference to issue number and date of capability manual;

  ii) programme for capability approval;
  iii) test results obtained during the programme;
  iv) abstract of description of capability;
  v) programme of maintenance of capability.

3.6.3.2 *Maintenance of capability approval*

3.6.3.2.1 Capability approval shall be maintained through lot-by-lot tests and periodic tests as prescribed for quality conformance inspection by the detail specification.

3.6.3.2.2 The manufacturer shall satisfy the NSI:

a) that the selection of CQCs remains representative of the circuits released and in accordance with the structural similarity rules prescribed in the sectional specification;

b) that the maintenance of capability programme continues to meet the requirements of the appropriate groups of the periodic testing and includes, where applicable, the requirements of any process test vehicle;

for each test sequence, the CQCs selected according to the structural similarity rules as representative of current circuits released, shall each be taken in the number prescribed for that test sequence;

c) that the limits of the capability have been successfully re-assessed in accordance with periodic testing within the 12 months following initial approval and every two years thereafter.

Note.- Approved limits extensions granted after initial approval require re-assessment on the same basis, related to their individual approval dates.

3.6.3.2.3 The manufacturer shall have maintained continuous production, such that:

a) the processes specified in the capability manual, including any additions/deletions agreed with the NSI since initial approval and any sub-contracted processes, remain unchanged;

b) there has been no change in the place of manufacture including sub-contracted processes and final test;

c) there has been no break exceeding six months in the manufacturer's declared maintenance of capability programme.

3.6.3.3 *Structural similarity*

The grouping of structurally similar circuits (including CQCs and process test vehicles) for the purpose of capability approval and quality conformance inspection shall be prescribed in the relevant sectional specification.

3.6.3.4 *Procedure in the event of failure in a periodic test*

The appropriate requirements of IEC Publication QC 001002 shall apply. The deficiency shall be corrected within six months. If this requirement cannot be fulfilled the capability approval shall be reduced accordingly.

3.6.3.5 *Changes in the approved capability*

It is the responsibility of the Chief Inspector to decide whether a change in material, process, procedure or capability is classified as a "major" one.

A record of all changes in materials and/or processes and procedures which may affect the quality of circuits shall be maintained. This data shall be made available to the NSI on request.

3.6.3.5.1 *Major changes*

When a change is required which either extends the scope of the approved capability or significantly affects the quality of the circuit(s), the manufacturer shall notify and agree on an incremental validation test programme with the NSI.

Upon its successful completion, the relevant specifications, the capability manual and, where appropriate, the scope of the approved capability, shall be amended as necessary.

3.6.3.5.2 *Other changes*

When the change is considered to be "not major", no formal approval tests are required, though the Chief Inspector may, at his discretion, request supporting data or tests to satisfy himself.

3.6.3.5.3 *Reduction in capability*

When a manufacturer wishes to reduce the scope of his approved capability, the NSI shall be satisfied that the amended capability manual and selection of CQCs and process test vehicles properly defined and assess the reduced scope.

3.6.4 *Capability manual*

The content of the capability manual shall be in accordance with the requirements of the relevant sectional specification.

The NSI shall treat the capability manual as a confidential document. The manufacturer may, if he wishes, disclose part or all of it to a third party.

3.7 Certified records of released lots

3.7.1 *General*

The requirements of IEC Publication QC 001002, Clause 14, shall apply.

3.7.2 *General requirements*

The manufacturer shall maintain records of released lots related to the lot-by-lot and periodic tests having the information contents detailed in Sub-clause 3.7.3. He may organize this data and make it available to customers in either of the following forms for each circuit or structurally similar group:

a) in one document available to NSI and to any customer;

b) in two documents, namely:

- for lot-by-lot tests (groups A and B) and periodic tests (sub-group D1) available to NSI and any relevant customer;
- the periodic tests (sub-groups C1 and D2) available to the NSI only.

3.7.3 *Content of Certified Records of Released Lots (CRRL)*

3.7.3.1 *Catalogue circuits (and CQCs if applicable)*

The following requirements are minimal and the detail specification may add further requirements. The manufacturer may, at his discretion, include explanatory notes and additional results provided that such additional results are complete and accurate:

a) lot-by-lot tests, sub-group A2 and Group B - attributes data;

b) periodic tests, sub-groups C1 to C4 - attributes data;

c) periodic tests, sub-group D1 - measurements data for each characteristic specified in the detail specification.

3.7.3.2 *Custom-built circuits*

Customers are advised to specify that Certified Records of Released Lots (CRRLs) should be provided for the period during which their circuits are manufactured.

3.8 Delayed deliveries

Circuits held for a period exceeding twelve months following the release of the lot shall be re-examined before delivery, for sub-group A2 and group B of the lot-by-lot test schedule. A period of two years is applicable to sub-group A1.

Once a "lot" has been satisfactorily re-inspected, its quality is re-assured for a further twelve months.

3.9 Delivery of F and HFICs subjected to destructive or non-destructive tests

Circuits subjected to tests indicated "destructive" (D) shall not be included in the lot for delivery.

Circuits subjected to "non-destructive" (ND) tests may be delivered provided they are re-tested according to the requirements of sub-groups A1 and A2 and group B of the lot-by-lot test schedule.

3.10 Supplementary procedure for deliveries

The manufacturer may at his discretion supply circuits that have met a higher assessment level than those being ordered.

3.11 Supplementary information

The detail specification may include information for application purposes which shall not be the subject of inspection within this specification.

SECTION 4 - TEST AND MEASUREMENT PROCEDURES

4.1 General

This section contains the library of tests which are applicable to F and HFICs.

The sectional specification or the detail specification shall prescribe which tests described in this section are applicable to a particular F and HFIC.

The sectional or the blank detail specification shall contain tables showing the tests to be performed, the measurements to be made before and after each test or subgroup of tests, and the sequence in which they shall be carried out. The tables shall also give information about the number of circuits to be tested, number of permissible defectives, and so on.

Where tests are prescribed in sequence, intermediate measurements may be omitted: the measurements made after the last test form the end point of the sequence.

Where tests are conducted in sequence the final measurements of one test may be taken as the initial measurements for the succeeding tests.

During measurements, the circuits shall not be exposed to draughts, direct sun-rays or other influences likely to cause error.

4.2 Standard conditions for testing

Unless otherwise prescribed, all tests and electrical measurements shall be carried out under standard conditions stated below.

4.2.1 *Standard atmospheric conditions*

4.2.1.1 *Standard atmospheric conditions for reference*

Temperature: 25 °C
Relative humidity: 50%
Air pressure: 101.3 kPa (1 013 mbar)

Note.- Air pressure is in accordance with IEC Publication 68-1. Temperature and relative humidity are in accordance with IEC Publication 749.

4.2.1.2 *Standard atmospheric conditions for referee tests*

(See IEC Publication 68-1, Sub-clause 5.1)

Temperature: 25 ± 1 °C
Relative humidity: between 48% and 52%
Air pressure: between 86 kPa and 106 kPa (between 860 mbar and 1 060 mbar)

Note.- The relative humidity may be disregarded where it has no influence on the test results.

4.2.1.3 *Standard atmospheric conditions for testing and for electrical measurements*

(See IEC Publication 68-1, Sub-clause 5.3)

Temperature: between 15 °C and 35 °C
Relative humidity: between 45% and 75%
Air pressure: between 86 kPa and 106 kPa (860 mbar and 1 060 mbar)

4.2.1.4 *Recovery conditions*

Temperature: actual laboratory temperature between 15 °C and 35 °C.
Relative humidity: between 45% and 75%
Air pressure: between 86 kPa and 106 kPa (860 mbar and 1 060 mbar)
Recovery time: 1 to 2 h, unless otherwise specified.

Note.- These conditions are in accordance with IEC Publication 68-1, Sub-clause 5.4.

4.2.2 *Definition of axis for mechanical tests*

Orientation

For those methods which involve observation or the application of external forces which shall be related to the orientation of the circuit, such orientations and direction of forces applied shall be in accordance with Figure 1. For other configurations the definitions of the axis shall be given in the detail specification.

Note.- The Y_1 force application is such that it will tend to lift the die off the substrate or the wires off the die.

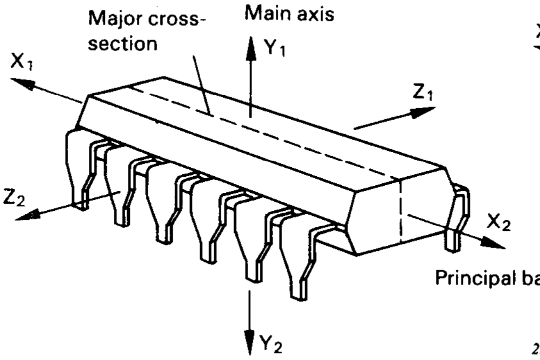

Fig. 1a. - Dual-in-line (DIL) package.

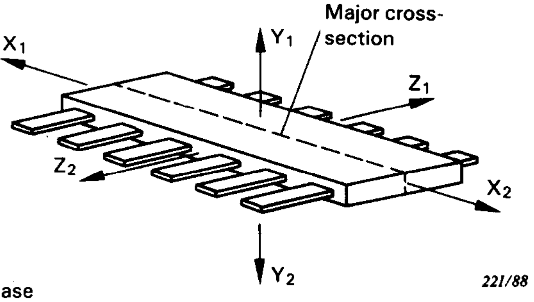

Fig. 1b. - Dual-in-line (DIL) package

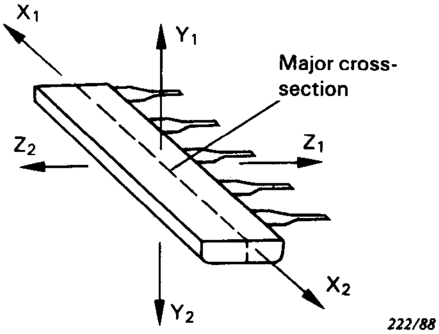

Fig. 1d. - Single-in-line package.

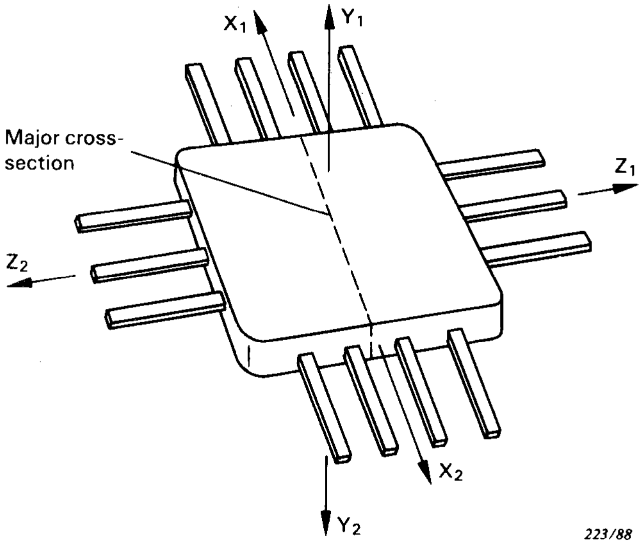

Fig. 1c. - Flat package with radial leads.

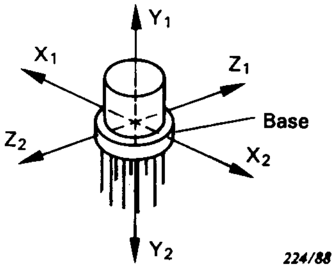

Fig. 1e. - Cylindrical package.

FIGURE 1

4.3 Visual examination

4.3.1 *Precap visual examination*

Under consideration.

4.3.2 *External visual and marking examination*

Unless otherwise specified, visual examination shall be performed under approved factory lighting conditions and under normal viewing conditions.

Inspection shall include the following items:

- marking and its legibility;
- terminal identification;
- appearance (e.g. broken encapsulation, cracks, and so on). For this test, a magnification of up to 10 x may be used for reference inspections.

4.3.3 *Dimensions*

The dimensions to be checked shall be those given in the reference drawing or in the detail specification.

4.4 Electrical measurement procedures

4.4.1 *Ratings*

The test conditions for all measurements shall be such that the maximum ratings of the circuits are not exceeded.

4.4.2 *Equilibrium conditions*

All electrical tests shall be conducted under equilibrium conditions unless otherwise specified or unless the measurement is being carried out under pulsed conditions. When test conditions cause significant change with time of the characteristic being measured, means of compensation for such effects shall be specified; for example, the length of time that the circuit shall be maintained at test conditions before making a measurement.

4.4.3 *Temperature*

The ambient temperature shall be measured as the air temperature adjoining the circuit in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.

4.4.4 *Precautions*

The precautions should include limits on maximum instantaneous currents and applied voltages. It is recommended that circuits should not be inserted into, or removed from, a test circuit while the latter is energized.

For electrostatic sensitive circuits, adequate precautions should be taken to prevent damage from static charges both before and after tests.

4.4.5 *Measurement circuit requirements and accuracy*

4.4.5.1 *Constant-current source*

A current shall be considered constant if a two-to-one increase of the effective load impedance does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement.

4.4.5.2 *Current-measuring device*

The effective admittance of a current-measuring device shall be sufficiently high so that halving its value does not significantly affect the accuracy of the measurement.

4.4.5.3 *Constant-voltage source*

A voltage shall be considered constant if a two-to-one decrease of the effective load impedance does not produce a change in the parameter being measured that is greater than the required accuracy of measurement.

4.4.5.4 *Voltage-measuring device*

The effective impedance of a voltage-measuring device shall be sufficiently high so that halving its value does not significantly affect the accuracy of measurement.

4.4.5.5 *Load impedance*

The load impedance represents the equivalent input impedance of the test circuit and the device under test. For acceptance test purposes, the input impedance may be replaced by a resistor representing worst case conditions.

4.4.5.6 *Power supplies*

The sources of direct currents and voltages shall not have a ripple content large enough to affect the desired accuracy of measurement. Test or supply voltages or currents shall be within ±1% of the specified value.

4.4.5.7 *Accuracy of measurements*

Unless otherwise specified, the accuracy of the measuring equipment shall be such that the error does not exceed:

a) for absolute measurements, 10% of the specified tolerance;

b) for relative measurements, 10% of the specified maximum change.

4.4.6 *Circuits with functionally independent sections*

Each functionally independent section of a circuit shall be tested individually and all terminals associated solely with sections not under test shall be left unconnected or as specified. Circuits shall be checked to ensure that interaction is not present between functionally independent sections.

Each of a group of functionally equivalent signal terminals shall be tested individually, with connections as specified in the detail specification applied to the remainder.

4.4.7 *Unspecified connections to terminals*

Any terminal for which no conditions are specified shall be left unconnected.

4.4.8 *Electrical measuring methods*

Measurements may be carried out by using the methods as prescribed in the sectional specification or any other method, giving compatible results but, in case of conflict, the specified method shall be used.

Note.- By "compatible" is meant that the value of the characteristic established by such other method will fall within the specified limits when measured by the specified method.

4.4.9 *Insulation resistance*

Unless otherwise prescribed in the detail specification, a d.c. voltage of 100 ± 15 V shall be applied for 1 min ± 5 s. Where necessary, the polarity shall be specified in the detail specification.

4.4.9.1 *Insulation between terminals (or groups of terminals)*

The voltage shall be supplied between any and every combination of terminals which are electrically and functionally isolated.

4.4.9.2 *Insulation between all the isolated terminals and the case*

The voltage shall be applied between a metal foil tightly held in contact with the case and all the terminals of the circuit connected together (except those leads which are electrically connected to the case). The size and positioning of the foil shall not reduce the insulation paths.

4.4.9.3 Unless otherwise specified in the detail specification, a circuit fails the test if there is:

a) evidence of flashover or mechanical damage;

b) any individual reading of insulation resistance less than 100 MΩ.

4.4.10 *Measurement of separately accessible elements*

4.4.10.1 *Deposited film elements*

4.4.10.1.1 *Deposited resistors*

The resistance value shall be measured with an absolute overall measurement system accuracy at least ten times better than the initial tolerance, when the initial tolerance is ±0.5% or greater.

An absolute overall measurement system accuracy at least five times better than the initial tolerance shall be required when the initial tolerance is less than ±0.5%.

Maximum power dissipation per resistor shall be 10% of the rated power or 0.01 W per resistor, whichever is less.

4.4.10.1.2 *Other deposited elements* (capacitors, crossovers, etc.)

The measurement of all deposited elements shall be achieved in accordance with IEC specifications, unless otherwise specified in the detail specification.

4.4.10.2 *Added components*

As in Sub-clause 4.4.10.1.2.

4.4.11 *Measurement of the electrical characteristics of the circuit*

Wherever possible, the tests shall be drawn from existing IEC standards.

4.5 Environmental testing procedures

The following tests are indicated "destructive" (D) or "non-destructive" (ND) according to their effect on the circuit.

Circuits subjected to tests indicated "destructive" (D) shall not be included in the lot for delivery, unless otherwise specified in the detail specification.

Circuits subjected to tests indicated "non destructive" (ND) may be delivered, provided they have satisfied group A requirements after re-testing.

4.5.1 *Storage at high temperature* (non-destructive)

When it is agreed that this test degrades solderability or other characteristics, the detail specification may either designate it as destructive or require it to be carried out in an inert atmosphere.

Initial measurements and visual examination: as applicable.

This test corresponds with Test Ba of IEC Publication 68-2-2 with the following details:

No special pre-conditioning procedure.

The air in the chamber need not be agitated and there shall be no requirement for relative humidity during the conditioning period.

Temperature: upper category temperature.

Duration of the conditioning after thermal equilibrium:

$$168^{+8}_{0}\text{ h},\ 336^{+8}_{0}\text{ h},\ 672^{+8}_{0}\text{ h or } 1\,000^{+8}_{0}\text{ h}$$

There shall be no loading or measurement performed during conditioning.

After the test, the circuits shall be allowed to recover for a maximum of 24 h (see Sub-clause 4.2.1.4).

The detail specification shall prescribe:

- temperature of conditioning;
- duration of conditioning;
- final measurements.

4.5.2 *Cold* (non-destructive)

Initial measurements and visual examination as applicable.

This test corresponds with Test Ab of IEC Publication 68-2-1, with the following details:

Temperature: lower category temperature.

There shall be no loading or measurements performed during conditioning.

After the test, the circuits shall be allowed to recover for a maximum of 24 h (see Sub-clause 4.2.1.4).

The detail specification shall prescribe:

- temperature of conditioning;
- duration of conditioning;
- final measurements.

4.5.3 *Damp heat, steady state* (destructive)

Initial measurements and visual examination as applicable.

This test corresponds with Test Ca of IEC Publication 68-2-3 with the following details:

No special pre-conditioning procedure.

Condition 1: temperature 40 ± 2 °C; relative humidity $93^{+2}_{-3}\%$
Condition 2: temperature 55 ± 2 °C; relative humidity 90 ± 5%
Condition 3: temperature 85 ± 2 °C; relative humidity 85 ± 5%

Duration: 4, 10, 21 or 56 days.

Other than bias (if required), there shall be no electrical loading or measurement performed during conditioning.

After the test, the circuits shall be allowed to recover for a maximum of 24 h (see Sub-clause 4.2.1.4).

The detail specification shall prescribe:

- test conditions 1, 2 or 3;
- duration of conditioning;
- bias if required;
- final measurements.

4.5.4 *Damp heat, cyclic* (destructive)

Initial measurements and visual examination: as applicable.

This test is in accordance with Test Db of IEC Publication 68-2-30 with the following details:

No special pre-conditioning procedure.

During conditioning: no loading, no measurements.

After the test, the circuits shall be allowed to recover for a maximum of 24 h (see Sub-clause 4.2.1.4)

The detail specification shall prescribe:

- upper temperature;
- number of cycles;
- final measurements.

4.5.5 *Shock* (non-destructive, unless otherwise stated in the detail specification)

Initial measurements and visual examination: as applicable.

This test is in accordance with Test Ea of IEC Publication 68-2-27 using the degree of severity prescribed in the detail specification.

Mounting: clamping both the body and the leads.

Gravitational effect: no special requirements.

Functioning: non-operative.

After the test the following requirements shall be met as prescribed in the detail specification:

- sealing as end point, if required;
- measurements and visual checks.

4.5.6 *Vibration, swept frequency* (destructive)

Initial measurements and visual examination: as applicable.

This test is in accordance with Test Fc of IEC Publication 68-2-6 using the method of mounting prescribed in the detail specification.

Test procedure: endurance by sweeping.

Severity to be selected from the following:

Condition	Frequency range	Acceleration	
	Hz	m/s²	Equivalent values g_n
1	150 - 2 000	196	(20)
2	55 - 500	98	(10)
3	20 - 150	49	(5)

The total duration shall be 20 sweep cycles in each of three mutually perpendicular directions.

Functioning: non-operative.

After the test, the following requirements shall be met as prescribed in the detail specification:

- sealing as end point, if required;
- measurement and visual checks.

4.5.7 *Acceleration, steady state* (non-destructive)

Initial measurements and visual examination: as applicable.

This test is in accordance with Test Ga of IEC Publication 68-2-7 using the method of mounting prescribed in the detail specification.

Direction of acceleration: to be applied to the most critical orientation.

Acceleration severity shall be chosen from the following:

Acceleration	
m/s²	Equivalent values g_n
294 000	30 000
196 000	20 000
98 000	10 000
49 000	5 000
19 600	2 000
4 900	500
490	50

Duration: The acceleration shall be increased to the specified value in not less than 20 s, remain at the specified acceleration for at least 1 min and then be decreased to zero in the same minimum time.

After the test, the following requirements shall be met as prescribed in the detail specification:

- sealing as end point, if required;
- measurements and visual checks.

4.5.8 *Change of temperature*

Initial measurements and visual examination: as applicable.

This test is in accordance with Tests Na, Nb or Nc of IEC Publication 68-2-14 with the following details:

4.5.8.1 *Test Na* (two chamber method, non-destructive)

Low temperature: T_{stg} min. ± 3 °C as prescribed in the detail specification.

High temperature: T_{stg} max. ± 3 °C as prescribed in the detail specification.

Functioning: non-operative.

Transfer temperature: 25 ± 5 °C.

Recovery: 2 h minimum and 4 h maximum.

After the test, the requirements for measurements and visual examination shall be met as prescribed in the detail specification.

4.5.8.2 *Test Nb* (one chamber method, non-destructive)

Low temperature: T_{stg} min. ± 3 °C as prescribed in the detail specification.

High temperature: T_{stg} max. ± 3 °C as prescribed in the detail specification.

The rate of change of temperature shall be 5 °C/min.

Number of cycles: 2, unless otherwise prescribed in the detail specification.

After the test, the requirements for measurements and visual examiation shall be met as prescribed in the detail specification.

Functioning: non-operative.

Recovery: 2 h minimum and 4 h maximum.

4.5.8.3 *Two-bath method*

Test Nc (two-bath method - non-destructive for cavity circuits, unless otherwise specified in the detail specification)

Low and high temperatures in accordance with IEC Publication 68.

Immersion time at low and high temperatures: 15 s for mass ≤ 15 g,
5 min for mass >15 g.

Transfer time: 3 s for mass ≤ 15 g,
10 s for mass >15 g.

Number of cycles: 10.

Recovery: droplets of water may be removed by a blast of clean dry air before the recovery period.

After the test, the requirements for measurements and visual examination shall be met as prescribed in the detail specification.

4.5.9 *Sealing* (non-destructive)

4.5.9.1 *Fine leak, tracer gas (helium) method with mass spectrometer*

This test is in accordance with test Qk of IEC Publication 68-2-17.

4.5.9.1.1 *Test method 1* (for circuits not filled with helium during manufacture)

After the test, the following limits of permissible equivalent standard leakage rate shall be met (unless otherwise prescribed in the detail specification):

- For circuits with an internal cavity volume of 0.1 cm^3 or less:
  maximum 5×10^{-8} $Pa.m^3/s$ (5×10^{-7} $bar.cm^3/s$) of dry air.
- For circuits with an internal cavity volume greater than 0.1 cm^3:
  maximum 5×10^{-7} $Pa.m^3/s$ (5×10^{-6} $bar.cm^3/s$) of dry air.

4.5.9.1.2 *Test method 2* (for circuits filled with helium during manufacturing)

After the test, the following limits of permissible equivalent standard leakage rate shall be met (unless otherwise prescribed in the detail specification:

- For circuits with an internal cavity volume of 0.1 cm^3 or less:
  maximum 5×10^{-8} $Pa.m^3/s$ (5×10^{-7} $bar.cm^3/s$) of dry air.

- For devices with an internal cavity volume greater than 0.1 cm^3: maximum 5 x 10^{-7} $Pa.m^3/s$ (5 x 10^{-6} $bar.cm^3/s$) of dry air.

4.5.9.2 *Gross leak-bubble test* (non-destructive)

This test is in accordance with Test Qc, Method 2 of IEC Publication 68-2-17.

The purpose of this method is to determine leakage rates larger than:

$$10^{-7}\ Pa.m^3/s$$

Type of test liquid:	A high boiling point liquid, for example, fluorocarbon.
Temperature of test liquid:	125 ± 5 °C or maximum storage temperature, whichever is less.
Volume of liquid:	The volume of liquid shall be sufficient so that the insertion of the circuit has no significant effect on the temperature.
Immersion:	The circuits shall be immersed to a depth of 50 mm minimum and remain in the liquid for a minimum of 30 s while being examined for the presence of bubbles.
Orientation:	For dual-in-line pack and flat-pack circuits, the caps shall be uppermost; for all other packages, the leads shall be uppermost.
Recovery:	After test, the circuits shall be removed from the liquid and cleaned of all traces of the liquid by means of a suitable water and solvent rinse procedure and dried in a warm air stream.
Requirement:	During the test, there shall be no continuous stream of bubbles from one or more locations on the circuits.

4.5.10 *Solderability* (destructive)

Initial measurements and visual examination as applicable.

These tests are destructive, except where the lead finish if not materially altered by the solderability tests or in the case of circuits to be shipped, the customer is prepared to accept the solderability test samples. Use of electrical rejects is permitted.

When considered necessary, accelerated ageing may be specified prior to the test.

The detail specification shall prescribe the ageing conditions, if applicable.

This test is in accordance with Test Ta of IEC Publication 68-2-20 with the following details:

4.5.10.1 *Solder bath method* (Test Ta, Method 1)

This test is in accordance with IEC Publication 68-2-20, Subclause 4.6.

Fluxing:	Prior to the test, the terminations shall first be immersed into a flux consisting of 25% by weight of colophony with 75% by weight of isopropanol, for a minimum time of 5 s to the depth as given below.
Immersion depth:	Up to the seating plane if any exists, otherwise to a point $2^{+0.5}_{0}$ mm from the body of the component.
Temperature:	235 ± 5 °C.
Duration:	2 ± 0.5 s.

When observed under 10 x magnification, the dipped surface shall be covered with a smooth and bright coating with no more than traces (approximately 10%) of scattered imperfections such as pin-holes or un-wetted areas. These imperfections shall not be concentrated in one area.

4.5.10.2 *Solder globule method* (Test Ta, Method 3)

This test is in accordance with IEC Publication 68-2-20, Subclause 4.8.

Fluxing:	The terminations shall be immersed into a flux consisting of 25% by weight of colophony with 75% by weight of isopropanol for a minimum time of 5 s.
Point of application:	5 ± 1 mm from the body.
Lead selection:	When applicable, two leads on each circuit comprising the sample shall be tested. The leads shall be selected in a cyclic manner, lead numbers 1 and 2 on the first circuit, numbers 2 and 3 on the second circuit and so on.
Requirement:	The solder shall wet the lead within 2,5 s.

4.5.11 *Resistance to soldering heat* (destructive)

Initial measurements and visual examination as applicable.

This test is in accordance with Test Tb, Method 1A or 1B of IEC Publication 68-2-20 with the following details:

A heat shield may be used where it is specified in the detail specification.

Immersion depth:	Up to the seating plane if any exists, otherwise to a point $2^{+0.5}_{0}$ mm from the body of the component.
Conditions:	260 ± 5 °C during 5 ± 1 s or 10 ± 1 s
or:	350 ± 10 °C during 3.5 ± 0.5 s.

The detail specification shall prescribe the requirements which are to be applied after the test.

4.5.12 *Robustness of terminations*

No more than five terminations need to be tested, but every position shall be tested on at least three circuits.

Initial measurements and visual inspection: as applicable.

Electrical rejects may be used.

4.5.12.1 *Tensile (pull test)* (destructive)

Electrical rejects may be used.

This test is in accordance with Test Ua_1 of IEC Publication 68-2-21.

The applied force shall be as prescribed in the detail specification.

4.5.12.2 *Thrust (push test)* (destructive)

This test is in accordance with Test Ua_2 of IEC Publication 68-2-21.

This test is performed only on those leads which support thrust when the circuit is being mounted.

The applied force per lead shall be as prescribed in the detail specification.

4.5.12.3 *Bending* (destructive)

This test is in accordance with Test Ub, Method 2, of IEC Publication 68-2-21.

4.5.12.3.1 *Wire or strip terminations*

Test Ub, Method 2, Sub-clause 4.5.2.1 applies.

Number of bends: two bends in one direction.

4.5.12.3.2 *Row of terminations* (simultaneous bending)

This test is in accordance with Test Ub. It is applicable to rows of terminations that are not intended to be bent by the user and/or preformed for mounting.

4.5.12.4 *Torque* (non-destructive)

This test is in accordance with Test Ud, Severity 1, of IEC Publication 68-2-21 with the following details:

The torque to be applied shall be prescribed in the detail specification.

4.5.12.5 *Torsion (wire termination only)* (destructive)

This test is in accordance with Test Uc of IEC Publication 68-2-21.

The degree of severity shall be prescribed in the detail specification.

4.5.12.6 *Requirements*

After each of these tests, the circuits shall be visually examined.

There shall be no visual damage.

After the conclusion of the last test, the measurements shall be made as prescribed in the detail specification.

4.5.13 *Salt mist* (destructive)

Initial measurements and visual examination: as applicable.

This test is in accordance with Test Ka of IEC Publication 68-2-11.

The test duration shall be as described in the detail specification.

After the test, the requirements for the measurements and the visual examination shall be met as prescribed in the detail specification.

4.5.14 *Electrical endurance test* (destructive, except when specified as a screening test, i.e. burn-in)

4.5.14.1 *General*

The test is described here by means of a reference test method in which a single circuit is tested in a test chamber capable of producing free air conditions. Actual methods of test are unlikely to conform exactly to the reference method. The Chief Inspector shall justify the method used, to the satisfaction of the NSI, as being not less severe than the reference method, having regard to the tests of IEC Publications 68-3-1 and 68-2-2.

The justification may relate to:

- the test chamber (see Sub-clause 4.5.14.2.1 below);
- the installation within the test chamber (see Sub-clause 4.5.14.2.2), including the installation of more than one circuit at one time;
- the evidence of continuity of test conditions if more than one circuit is installed.

4.5.14.2 *Reference test method*

Except where the detail specification prescribes any differences (in whole or in part), the following requirements shall apply:

4.5.14.2.1 *Test chamber*

The test shall take place in a test chamber equipped with an automatically-controlled means of maintaining a specified temperature and capable of producing free air conditions at a pressure of 100 ± 10 kPa (1.0 ± 0.1 bar), all in accordance with IEC publications, when a single circuit is installed therein as prescribed below.

4.5.14.2.2 *Installation*

The circuit shall be fitted with any accessories described in the detail specification as essential for operation at the power dissipation and temperature of the test.

The circuit shall be connected as necessary to wires of minimum practicable cross-section. In no case shall the metal section of a wire exceed that of the circuit terminal. Where possible, connection shall be made by soldering or welding. When this is not possible, the surface area of any connecting device shall be kept to a minimum.

The circuit shall be positioned in the chamber in accordance with IEC publications and with the normal mounting surface downward. Wherever possible, it shall be supported by the connecting wires only. If necessary, additional non-metallic string or fibre may be used to a minimum extent.

4.5.14.2.3 *Electrical operation*

Each section of the circuit shall, throughout the test, be subjected to an electrical programme representative of its intended function at the specified power dissipation and temperature of the total circuit.

The choice of power dissipation, operating temperature and supply voltage, shall be made in the following order of precedence:

a) The mean power dissipation in each functionally accessible section of the circuit shall be the maximum permitted by the detail specification.

b) The ambient or case temperature shall be the maximum permitted by the detail specification at the power dissipation of Item *a)*.

c) The supply voltages shall be the maximum permitted by the detail specification unless limited by Items *a)* and *b)*.

The mode of electrical operation shall be chosen from the following order of precedence:

d) Tests specified in the detail specification for the purpose of endurance testing.

e) Tests specified in the sectional specification for the purpose of endurance testing.

f) Tests specified in any IECQ generic or sectional specification appropriate to the functional type of circuit under test and intended for use in endurance testing.

g) An IEC test method normally used for endurance testing.

4.5.14.3 *Procedure*

4.5.14.3.1 *Pre-exposure measurements*

Test results for static and dynamic characteristics at room temperature and at the temperature extremes shall be available for the circuit, unless otherwise specified in the detail specification.

Results from any earlier testing which immediately precedes the endurance test may be used for this purpose. Test results may be attributes data for endurance tests of 168 h or less and shall be measurement data for tests of longer duration.

4.5.14.3.2 *Test exposure*

The circuit shall be installed in the chamber, the electrical operation shall be started, and the chamber temperature shall be raised until:

a) For ambient-rated circuits, the air temperature at a point 5 cm below the circuit reaches the specified level. The measuring probe shall not obstruct the air flow past the circuit and shall be shielded to eliminate any radiation effect from the circuit itself.

or

b) For case rated circuits, the temperature of the specified reference point on the surface of the circuit reaches the specified level.

The measuring probe shall be of the contacting type and shall not be capable of removing significant heat from the circuit.

Test exposure shall be considered to start when the ambient or reference-point temperature first reaches a value 2 °C below the specified value. Exposure shall thereafter continue without any deliberate interruption for the specified period.

Evidence shall be available to show that deviations from specified conditions have not exceeded the following limits:

c) The ambient or case temperature has remained within ±5 °C of the specified value, except that:

i) downward deviations not exceeding 10% of the temperature value, expressed in Celsius degrees, are permitted for a total period less than 10% of the test period;

ii) in the event of an upward deviation, the Chief Inspector shall decide whether the test should be abandoned.

d) The power dissipation of the circuit has remained within ±10% of the specified value.

Any deviation beyond these limits or any interruption of the electrical programme shall be classified as a temporary interruption to the test.

The total duration of temporary interruptions shall not exceed 20% of the test period.

Temporary interruptions shall not be credited to the test period.

Evidence of continuity of exposure shall be available to the NSI, preferably as continuous chart records (e.g., print-out from a data logger and from clocks on both oven and power supply), but acceptably from manual observations.

For tests of 168 h or less, observations shall be made at the start, finish and at least one intermediate point during the endurance period.

For tests of longer duration, the interval between periodic observations shall not exceed one week, with a minimum of nine intermediate observations, evenly spaced.

When periodic observations are used, the data recorded shall be considered to apply to the period half-way between the previous observation and the succeeding observation unless other evidence is available.

The records shall show, as a minimum:

- the temperature of the exposure (ambient or case temperature, as relevant);
- supply voltages;
- power dissipation;
- continuity of the electrical programme;
- date and time.

The records shall be retained by the manufacturer for a minimum period of three years after completion of the test.

4.5.14.4 *Post-test end-point measurements*

After any specified period of recovery, the post-test end-point measurements shall be a repetition of the pre-exposure measurement, prescribed in Sub-clause 4.5.14.3.1. Measurements may be made whilst the circuit is within the chamber or after removal at the manufacturer's discretion. If specified in the detail specification, circuits containing active elements shall be removed and shall be allowed to cool with the power still applied.

4.5.14.5 *Requirements of the detail specification*

The detail specification shall prescribe:

a) duration of the test;

b) electrical programme, supply voltage and power dissipation, either uniquely or by a reference;

c) ambient or reference-point temperature;

d) any installation or test condition which differs from those given in the reference test method;

e) recovery conditions;

f) CRRL requirements before and after the test.

4.5.15 *Resistance to solvents*

4.5.15.1 *Marking resistance to solvents* (non destructive)

The circuits shall be subjected to Test XA of IEC Publication 68-2-45, with the following details:

- Solvent to be used: see IEC Publication 68-2-45, Sub-clause 3.1.1.

  Solvent temperature: 23 ± 5 °C unless otherwise specified.

- Conditioning: Method 1 (with rubbing).
- Rubbing material: cotton wool.
- Recovery time: Not applicable, unless otherwise stated in the detail specification.

After the test, the marking shall be legible.

4.5.15.2 *Circuit resistance to solvents* (non destructive)

The circuits shall be subjected to Test XA of IEC Publication 68-2-45, with the following details:

- Solvent to be used: see IEC Publication 68-2-45, Sub-clause 3.1.1.
- Solvent temperature: 23 ± 5 °C unless otherwise specified.
- Conditioning: Method 2 (without rubbing).
- Recovery time: 10 min if weight measurement is required. In the other cases: 48 h, unless otherwise stated in the detail specification.

After the test, the requirements for the measurements shall be met as prescribed in the detail specification.

4.5.16 *Induced flammability* (destructive)

This test shall be carried out in accordance with IEC Publication 695-2-2 (needle flame test) with the appropriate severities as prescribed in the detail specification.